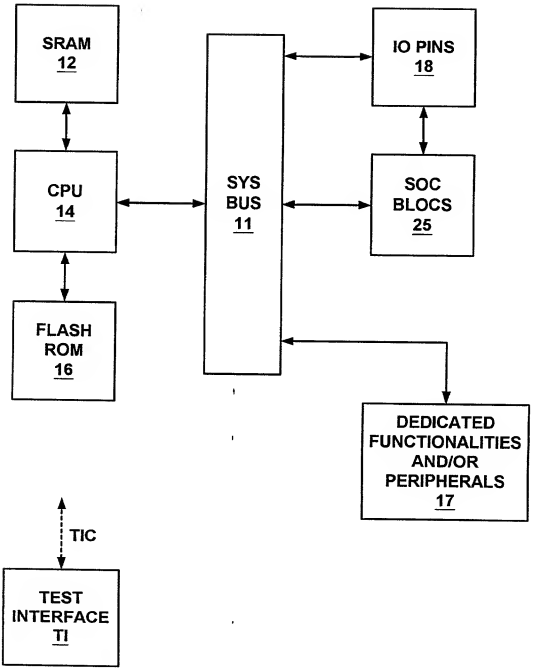


FIGURE 1A

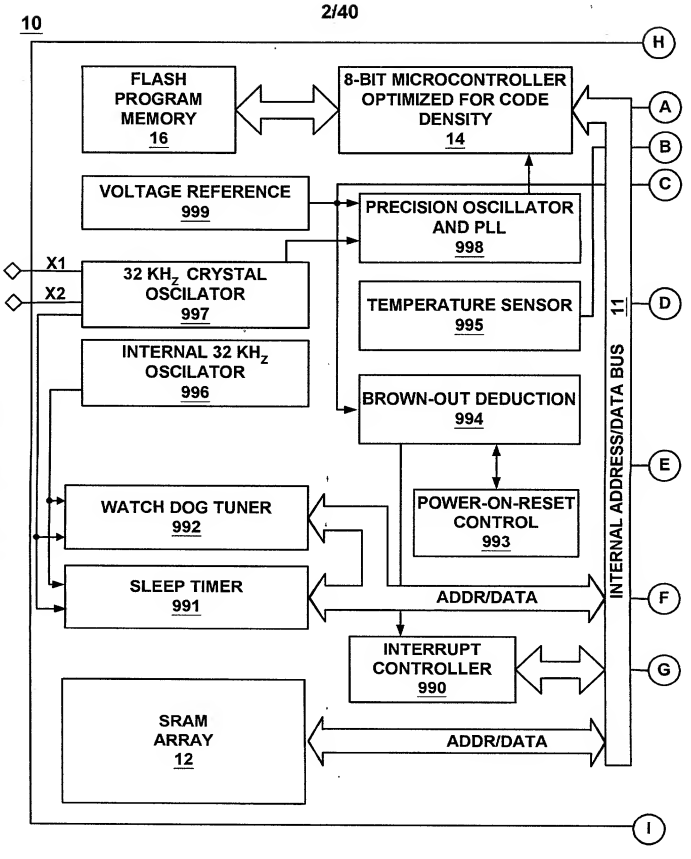


FIGURE 1B

10 (CONT.)

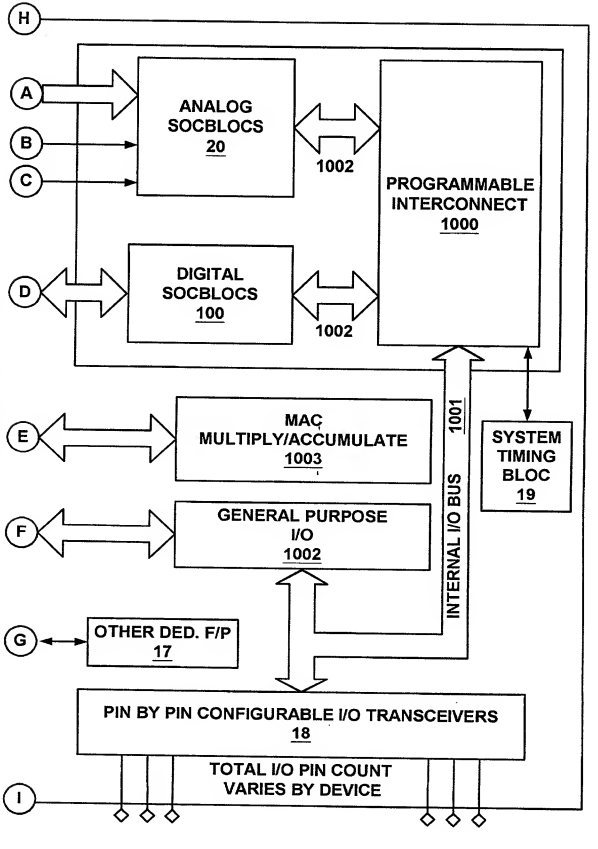


FIGURE 1B (CONT.)

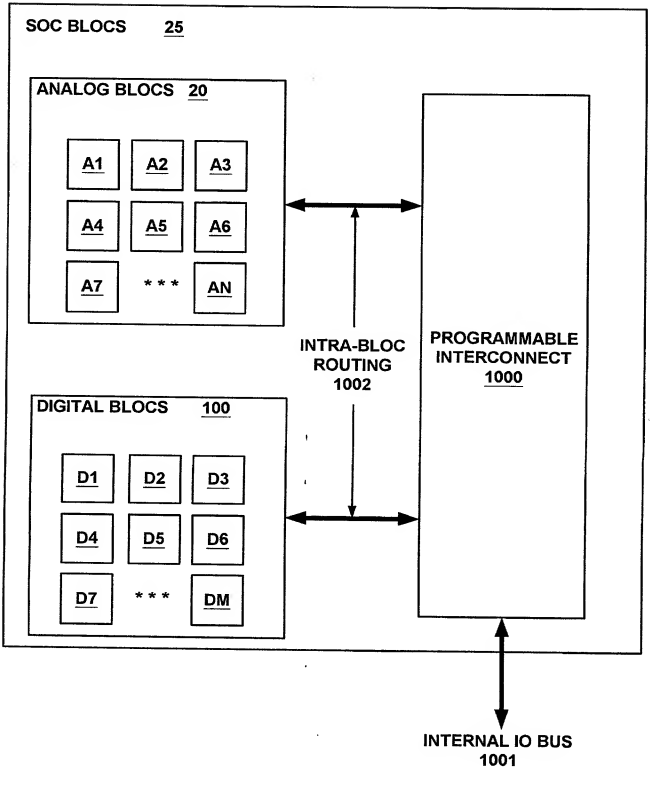


FIGURE 1C

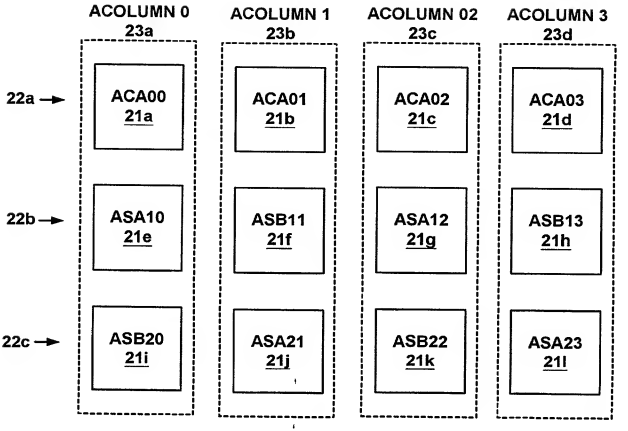


FIGURE 2

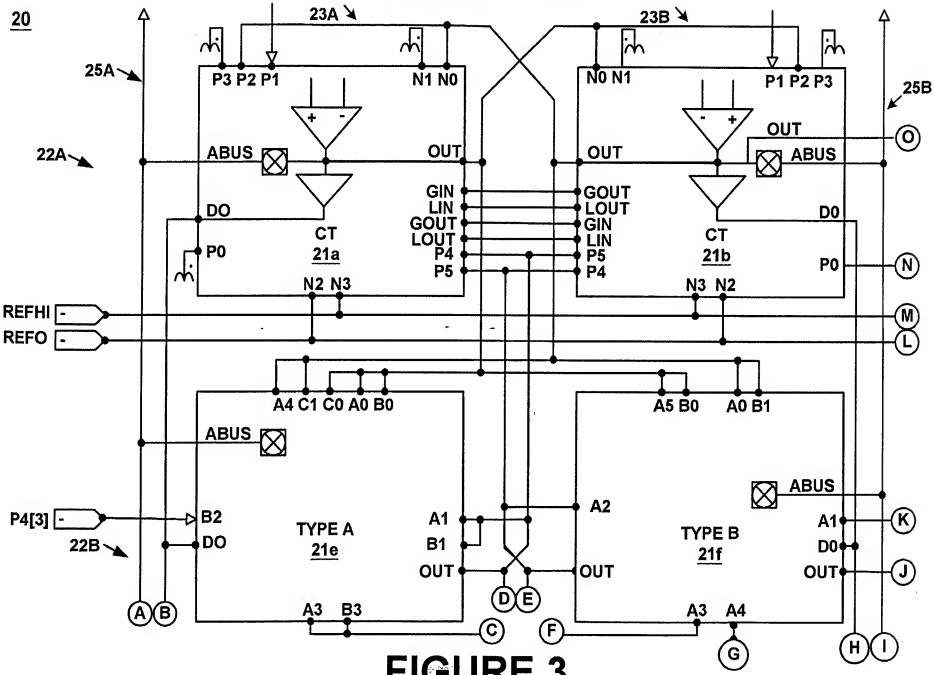

20
23A
23B
25A
25B
22A
P3 P2 P1
N1 N0
N0 N1
P1 P2 P3
ABUS
OUT
DO
D0
P0
CT
21a
21b
GIN
LIN
GOUT
LOUT
P4
P5
N2 N3
N3 N2
REFHI
REFO
A4 C1 C0 A0 B0
A5 B0
A0 B1
P4[3]
22B
B2
TYPE A
21e
TYPE B
21f
A1
B1
A2
A3 B3
A3 A4
A
B
C
D
E
F
G
H
I
J
K
L
M
N
O

FIGURE 3

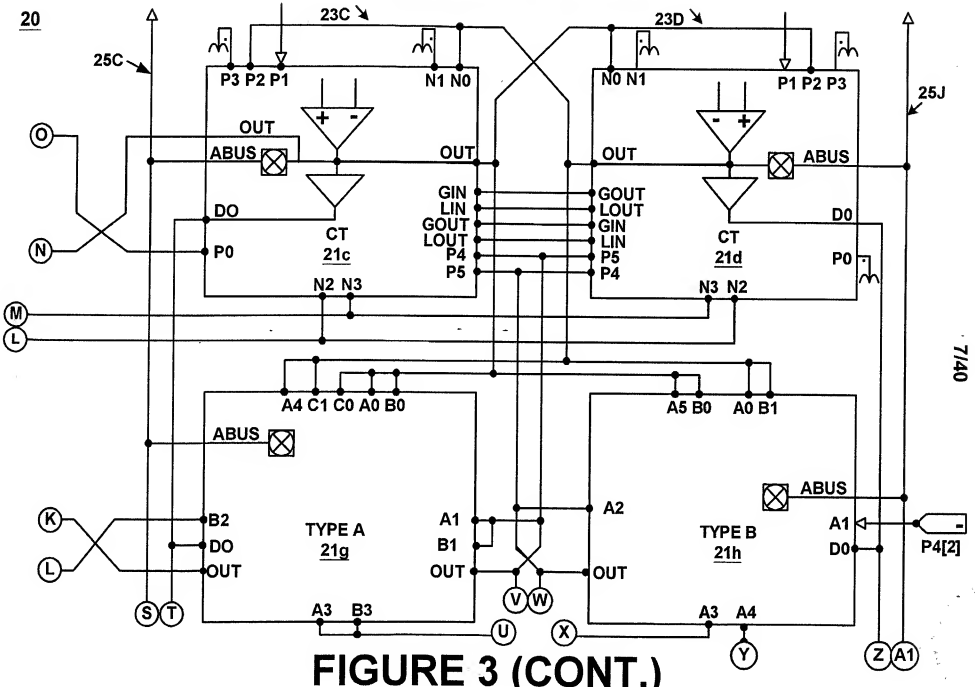


FIGURE 3 (CONT.)

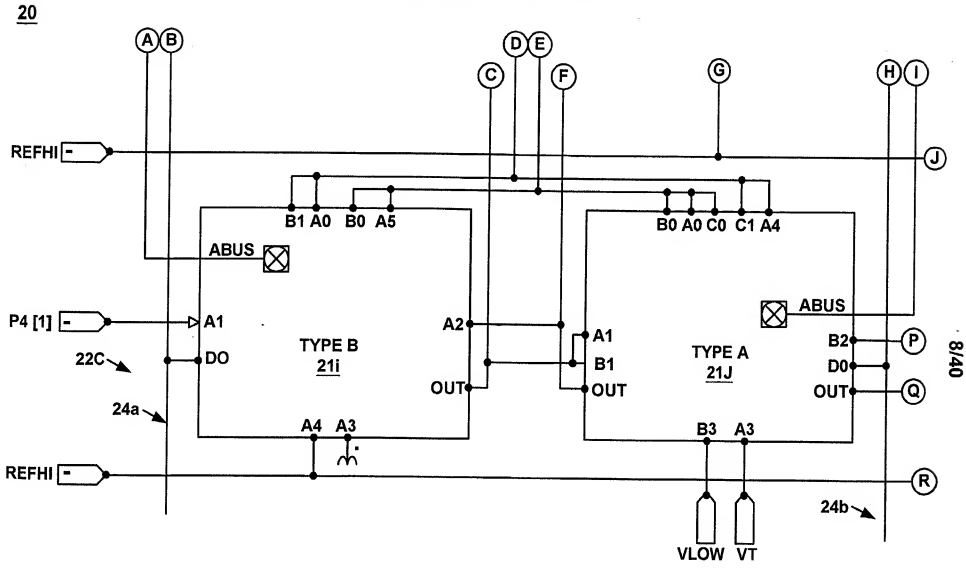


FIGURE 3 (CONT.)

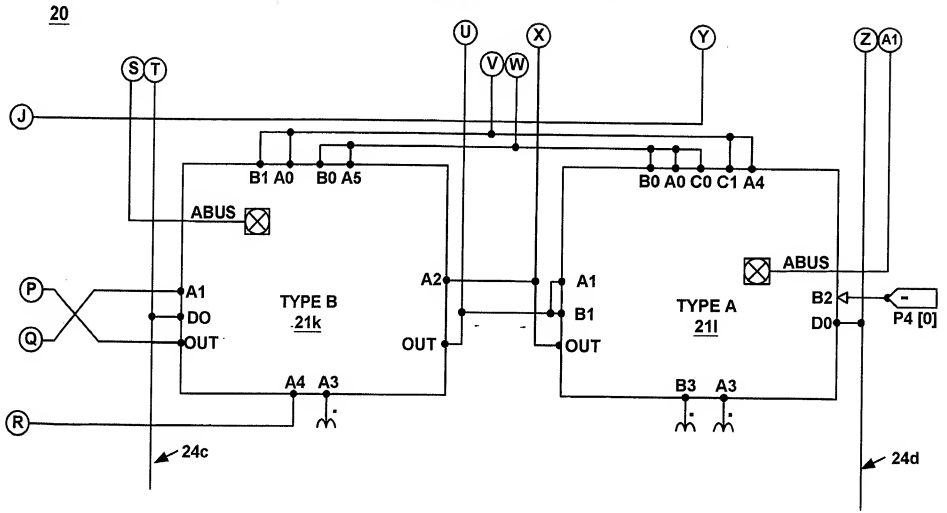


FIGURE 3 (CONT.)

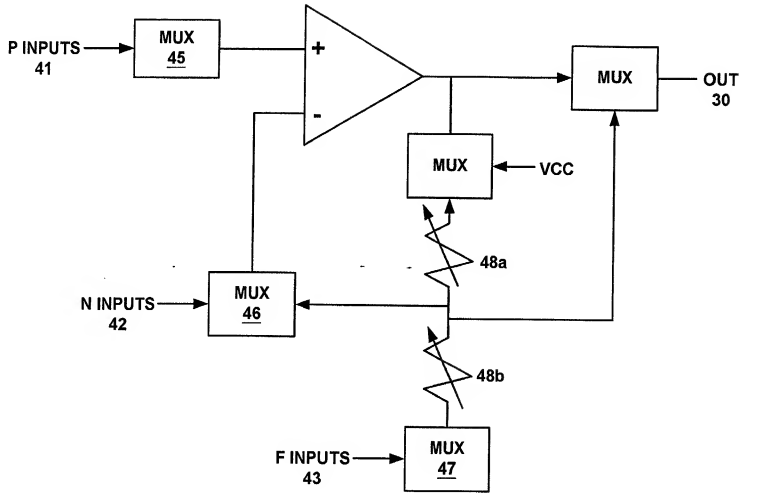

40
P INPUTS
41
MUX
45
+
-
MUX
OUT
30
MUX
VCC
48a
N INPUTS
42
MUX
46
48b
F INPUTS
43
MUX
47

FIGURE 4A

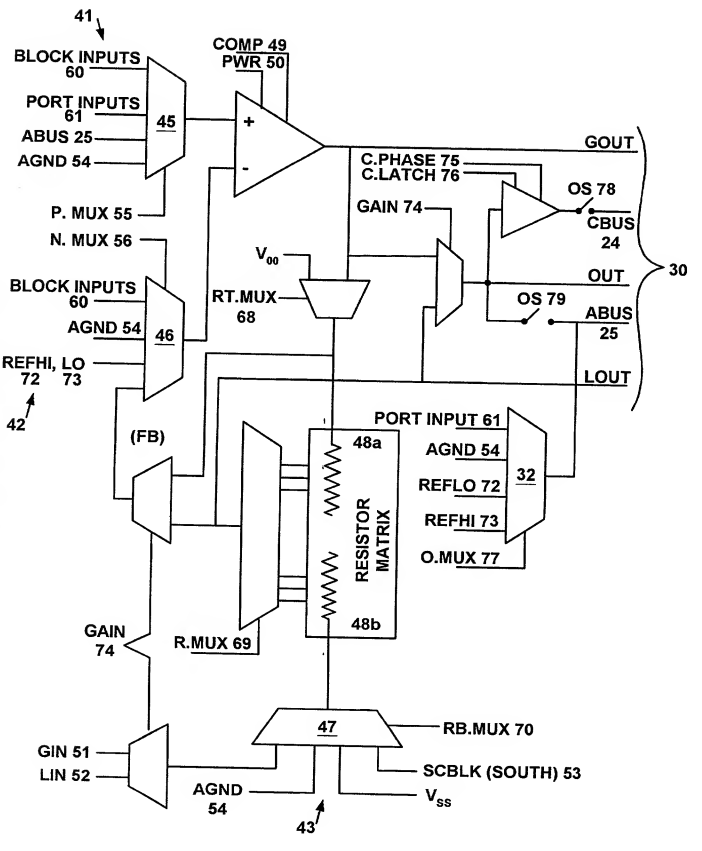

40
41
BLOCK INPUTS 60
PORT INPUTS 61
ABUS 25
AGND 54
45
P. MUX 55
N. MUX 56
BLOCK INPUTS 60
AGND 54
46
REFHI, LO 72 73
42
COMP 49
PWR 50
+
-
GOUT
C.PHASE 75
C.LATCH 76
OS 78
CBUS 24
GAIN 74
V_{00}
RT.MUX 68
OUT
OS 79
ABUS 25
LOUT
30
PORT INPUT 61
AGND 54
REFLO 72
REFHI 73
O.MUX 77
32
(FB)
48a
RESISTOR MATRIX
48b
GAIN 74
R.MUX 69
47
RB.MUX 70
GIN 51
LIN 52
AGND 54
SCBLK (SOUTH) 53
V_{SS}
43

FIGURE 4B

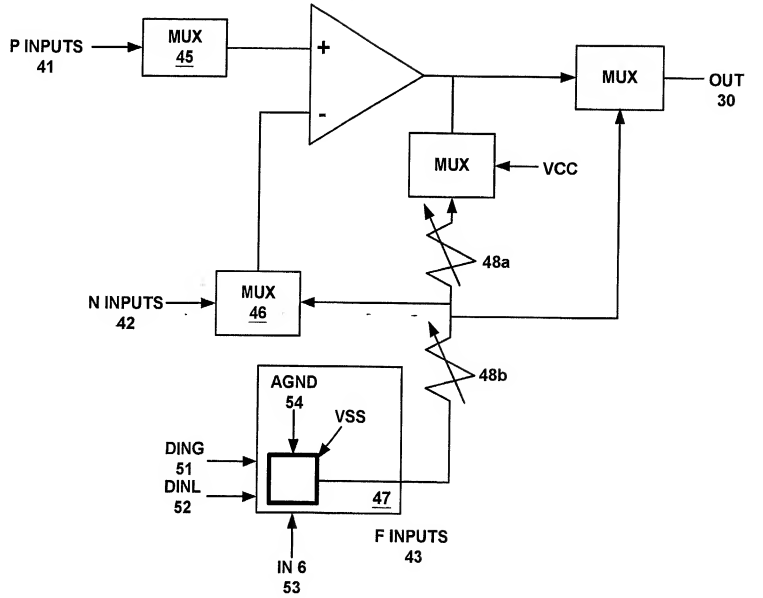

40
P INPUTS
41
MUX
45
+
-
MUX
OUT
30
MUX
VCC
48a
N INPUTS
42
MUX
46
48b
AGND
54
VSS
DING
51
DINL
52
47
F INPUTS
43
IN 6
53

FIGURE 5

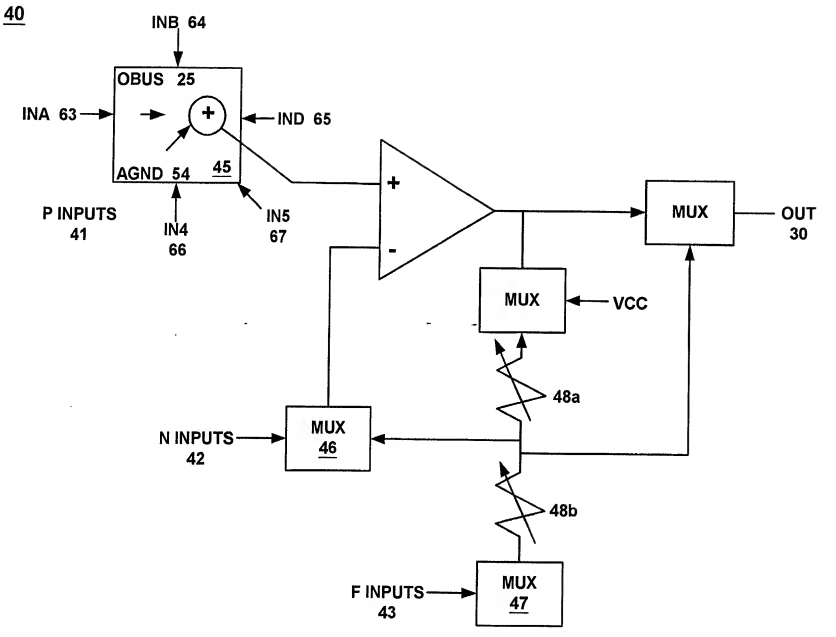

40
INB 64
OBUS 25
INA 63
IND 65
AGND 54
45
P INPUTS
41
IN4
66
IN5
67
+
-
MUX
OUT
30
MUX
VCC
48a
N INPUTS
42
MUX
46
48b
F INPUTS
43
MUX
47

FIGURE 6

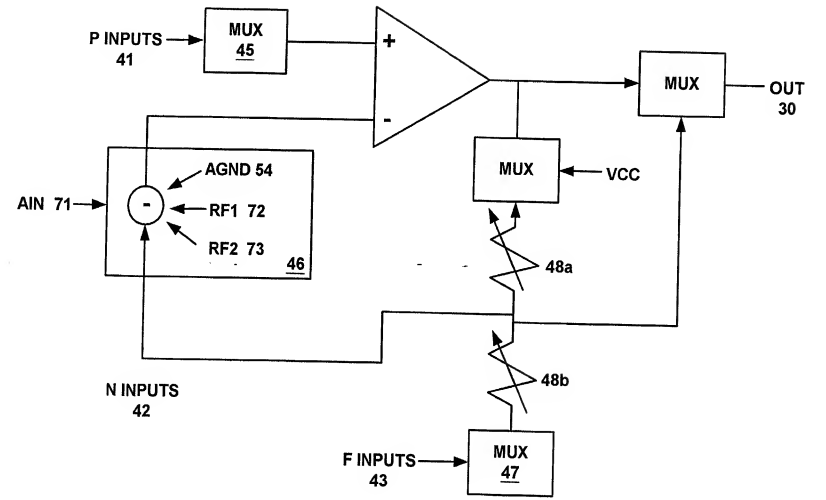
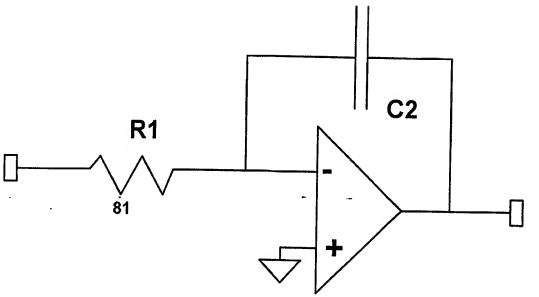

40
P INPUTS
41
MUX
45
+
-
MUX
OUT
30
MUX
VCC
AIN 71
AGND 54
RF1 72
RF2 73
46
48a
48b
N INPUTS
42
F INPUTS
43
MUX
47

FIGURE 7

80



$$\frac{1}{(R1C2)} \int V(t)\, dt$$

FIGURE 8A

85

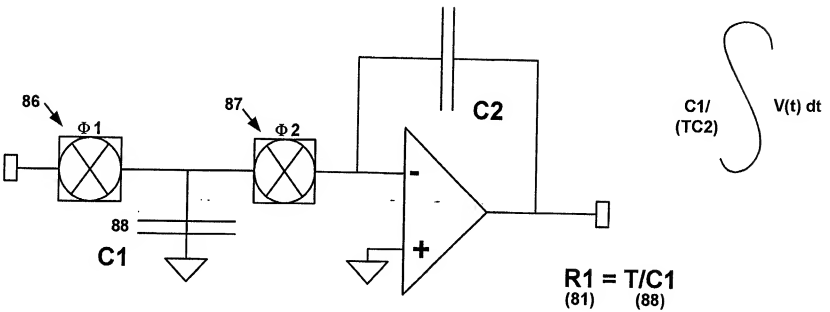


FIGURE 8B

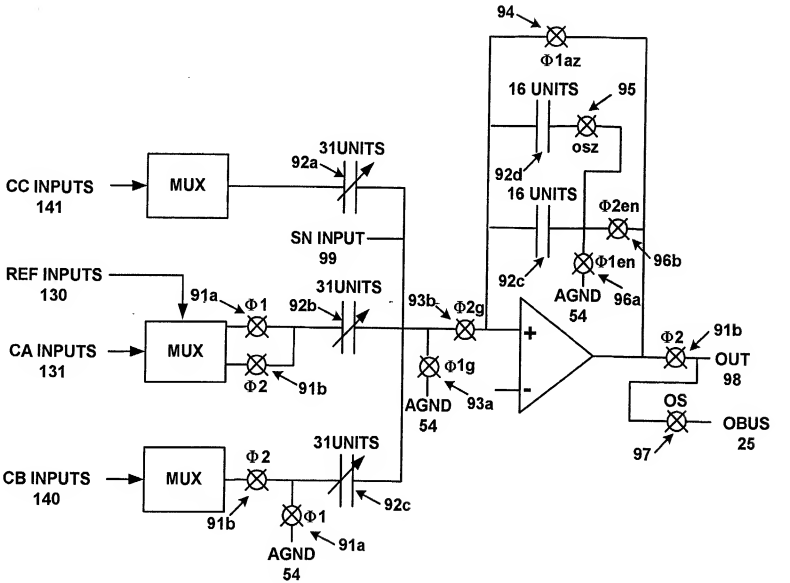

90
94
Φ1az
16 UNITS
95
osz
92d
16 UNITS
Φ2en
31UNITS
92a
CC INPUTS
141
MUX
SN INPUT
99
Φ1en
96b
92c
AGND
54
96a
REF INPUTS
130
91a
Φ1
31UNITS
92b
93b
Φ2g
Φ2
91b
CA INPUTS
131
MUX
Φ2
91b
Φ1g
AGND
54
93a
OUT
98
OS
OBUS
25
97
31UNITS
Φ2
CB INPUTS
140
MUX
92c
91b
Φ1
91a
AGND
54

FIGURE 9A

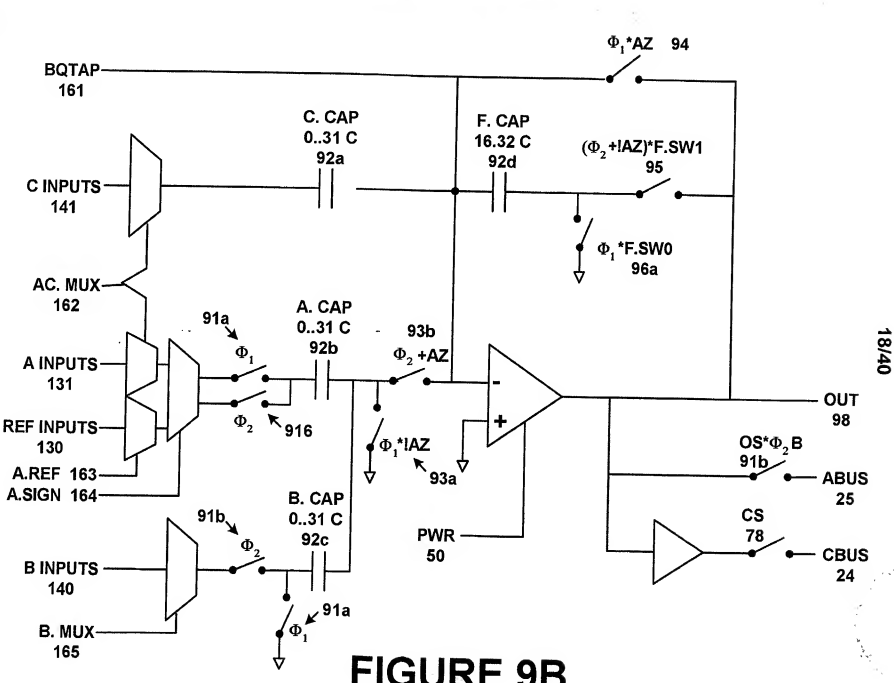

90a
BQTAP
161
Φ_1*AZ 94
C. CAP
0..31 C
92a
F. CAP
16.32 C
92d
(Φ_2+IAZ)*F.SW1
95
C INPUTS
141
Φ_1*F.SW0
96a
AC. MUX
162
91a
A. CAP
0..31 C
92b
93b
Φ_2 +AZ
A INPUTS
131
Φ_1
Φ_2
916
REF INPUTS
130
A.REF 163
A.SIGN 164
Φ_1*IAZ
93a
OUT
98
OS*Φ_2B
91b
ABUS
25
91b
B. CAP
0..31 C
92c
PWR
50
CS
78
CBUS
24
B INPUTS
140
Φ_2
91a
Φ_1
B. MUX
165

FIGURE 9B

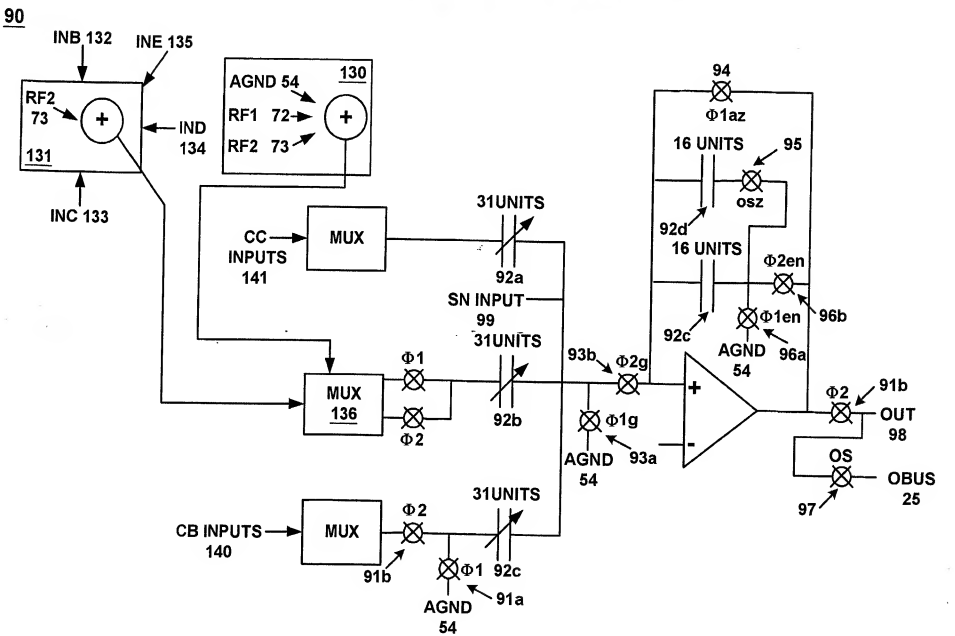

90
INB 132
INE 135
RF2
73
131
IND
134
INC 133
AGND 54
130
RF1 72
RF2 73
CC
INPUTS
141
MUX
31UNITS
92a
SN INPUT
99
MUX
136
Φ1
Φ2
31UNITS
92b
93b
Φ2g
Φ1g
AGND
54
93a
94
Φ1az
16 UNITS
95
osz
92d
16 UNITS
Φ2en
92c
Φ1en
96b
AGND
54
96a
Φ2
91b
OUT
98
OS
OBUS
25
97
CB INPUTS
140
MUX
Φ2
91b
Φ1
92c
AGND
54
91a
31UNITS

FIGURE 10

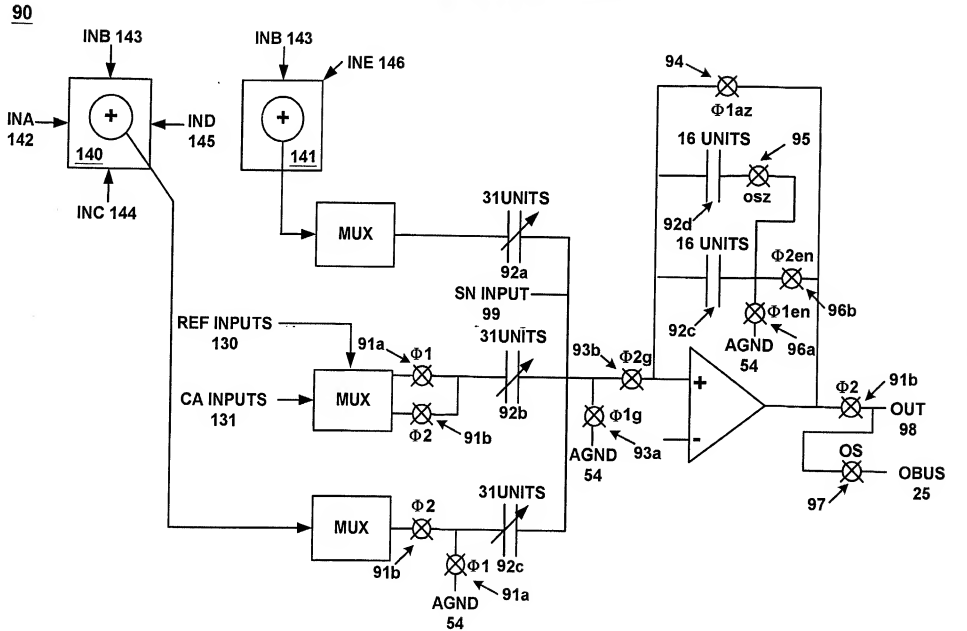

90
INB 143
INB 143
INE 146
INA 142
IND 145
140
141
INC 144
MUX
31UNITS
92a
SN INPUT 99
REF INPUTS 130
91a
Φ1
31UNITS
93b
Φ2g
CA INPUTS 131
MUX
92b
Φ2
91b
Φ1g
AGND 54
93a
MUX
Φ2
31UNITS
91b
Φ1
92c
AGND 54
91a
94
Φ1az
16 UNITS
95
osz
92d
16 UNITS
Φ2en
Φ1en
96b
92c
AGND 54
96a
Φ2
91b
OUT 98
OS
OBUS 25
97

FIGURE 11

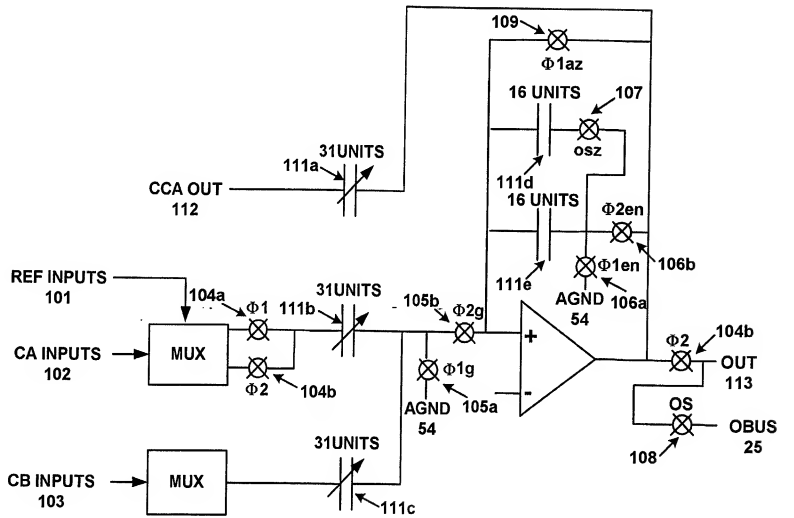

100
109
Φ1az
16 UNITS
107
osz
31UNITS
111a
CCA OUT
112
111d
16 UNITS
Φ2en
Φ1en
106b
REF INPUTS
101
104a
Φ1
31UNITS
111b
111e
AGND
54
106a
105b
Φ2g
CA INPUTS
102
MUX
Φ2
104b
Φ1g
AGND
54
105a
+
-
Φ2
104b
OUT
113
OS
OBUS
25
108
31UNITS
CB INPUTS
103
MUX
111c

FIGURE 12A

100a

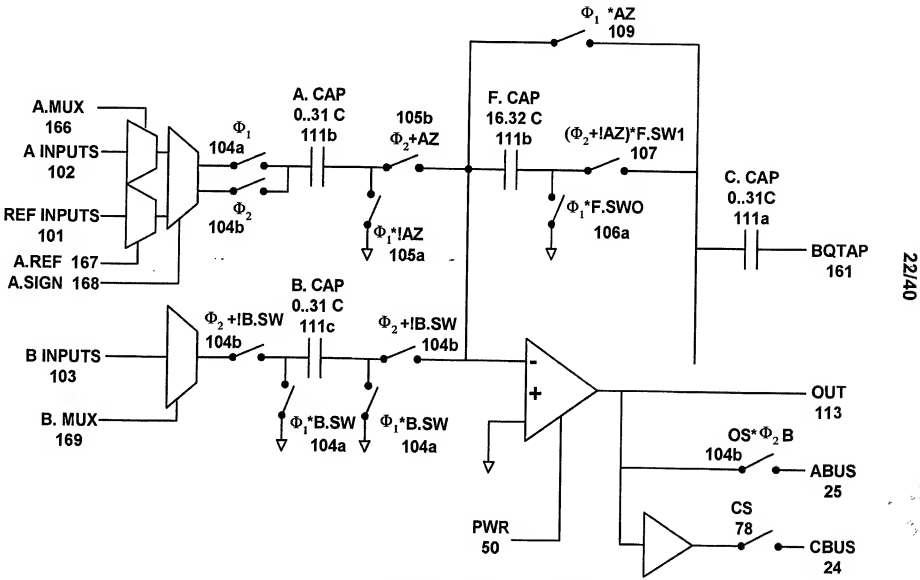


FIGURE 12B

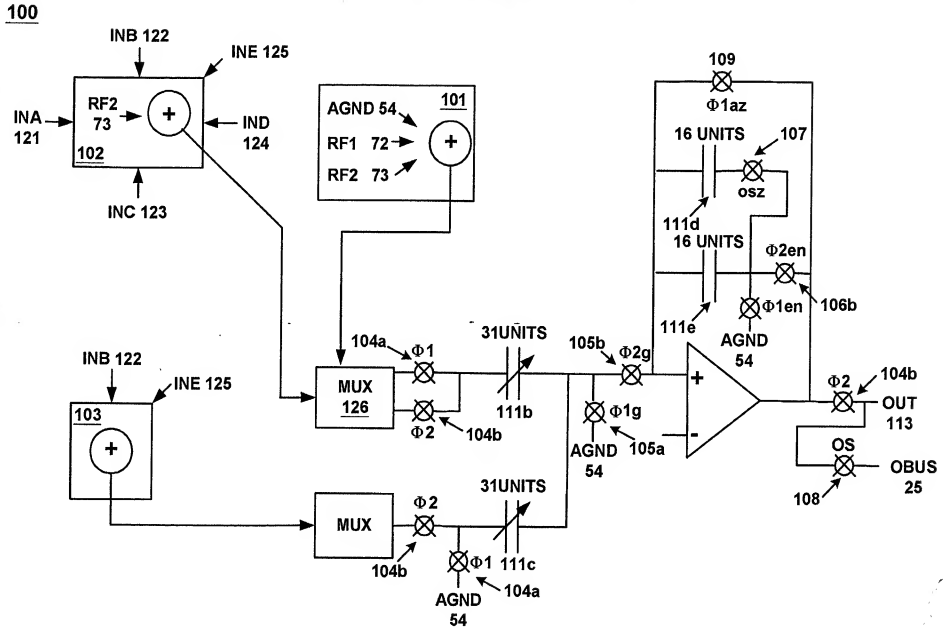

100
INB 122
INE 125
INA 121
RF2 73
IND 124
102
INC 123
AGND 54
101
RF1 72
RF2 73
109
Φ1az
16 UNITS
107
osz
111d
16 UNITS
Φ2en
Φ1en
106b
111e
AGND 54
104a
Φ1
31UNITS
105b
Φ2g
MUX 126
Φ2
104b
111b
Φ1g
AGND 54
105a
Φ2
104b
OUT 113
OS
OBUS 25
108
INB 122
INE 125
103
MUX
Φ2
31UNITS
104b
Φ1
111c
104a
AGND 54

FIGURE 13

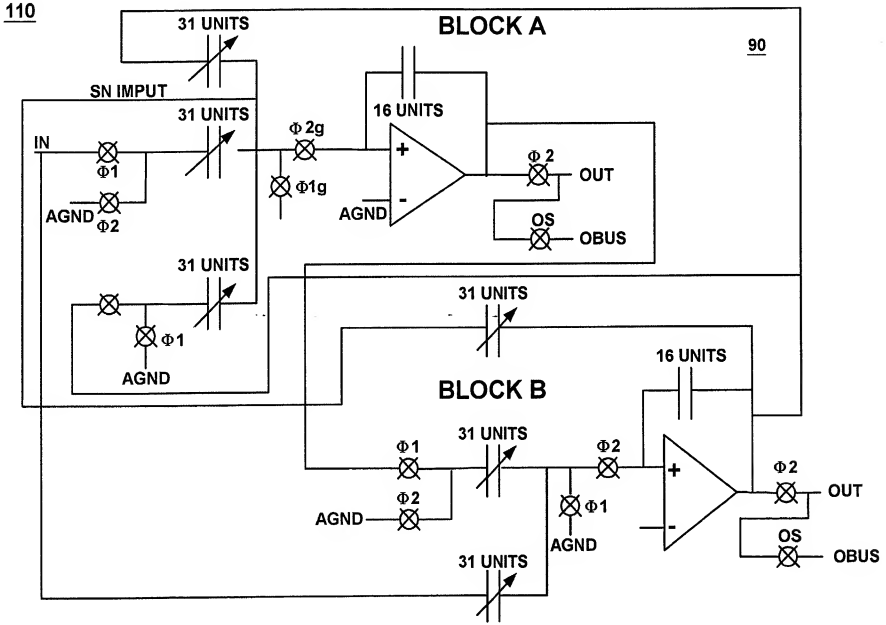

110
31 UNITS
BLOCK A
90
SN IMPUT
31 UNITS
16 UNITS
IN
Φ1
Φ2g
Φ2
OUT
AGND
Φ2
Φ1g
AGND
OS
OBUS
31 UNITS
31 UNITS
Φ1
AGND
16 UNITS
BLOCK B
Φ1
31 UNITS
Φ2
Φ2
OUT
AGND
Φ2
Φ1
AGND
OS
OBUS
31 UNITS

FIGURE 14A

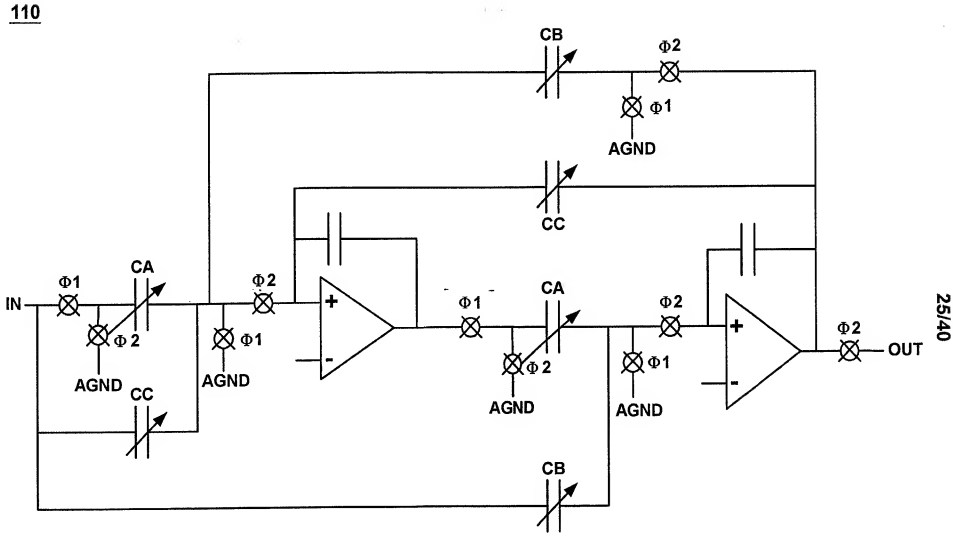

110
CB
Φ2
Φ1
AGND
CC
Φ1
CA
Φ2
IN
Φ2
Φ1
Φ2
CA
Φ2
Φ2
Φ2
OUT
AGND
AGND
CC
AGND
AGND
CB

FIGURE 14B

1500

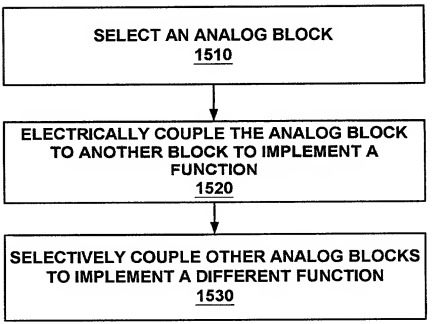


FIGURE 15

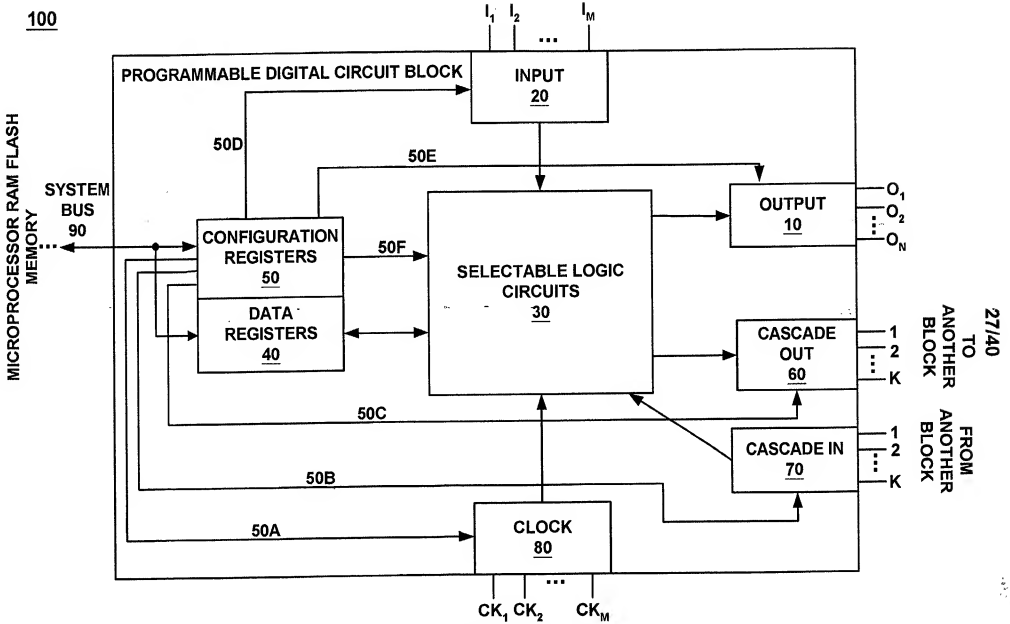


FIGURE 16

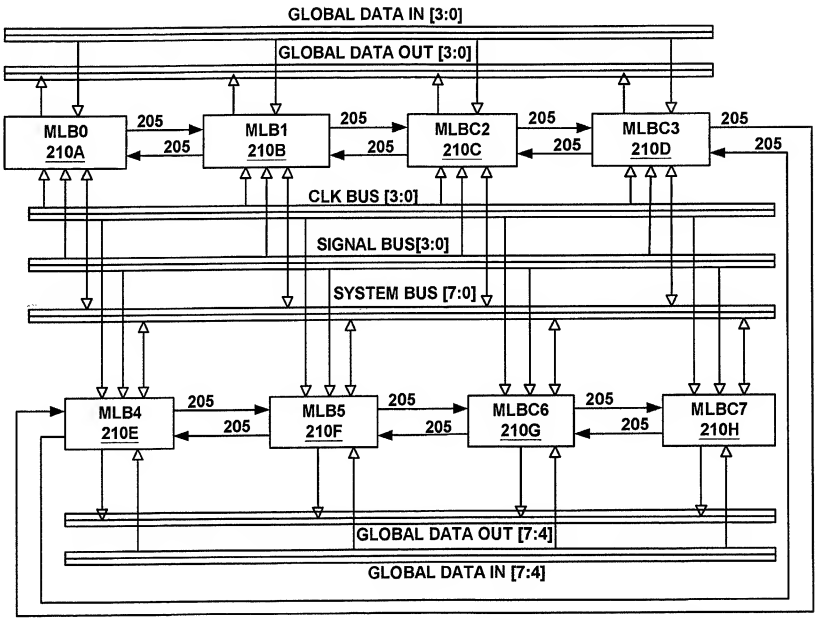

200
GLOBAL DATA IN [3:0]
GLOBAL DATA OUT [3:0]
MLB0 210A
MLB1 210B
MLBC2 210C
MLBC3 210D
205
CLK BUS [3:0]
SIGNAL BUS[3:0]
SYSTEM BUS [7:0]
MLB4 210E
MLB5 210F
MLBC6 210G
MLBC7 210H
GLOBAL DATA OUT [7:4]
GLOBAL DATA IN [7:4]

FIGURE 17

TIMER CONFIGURATION

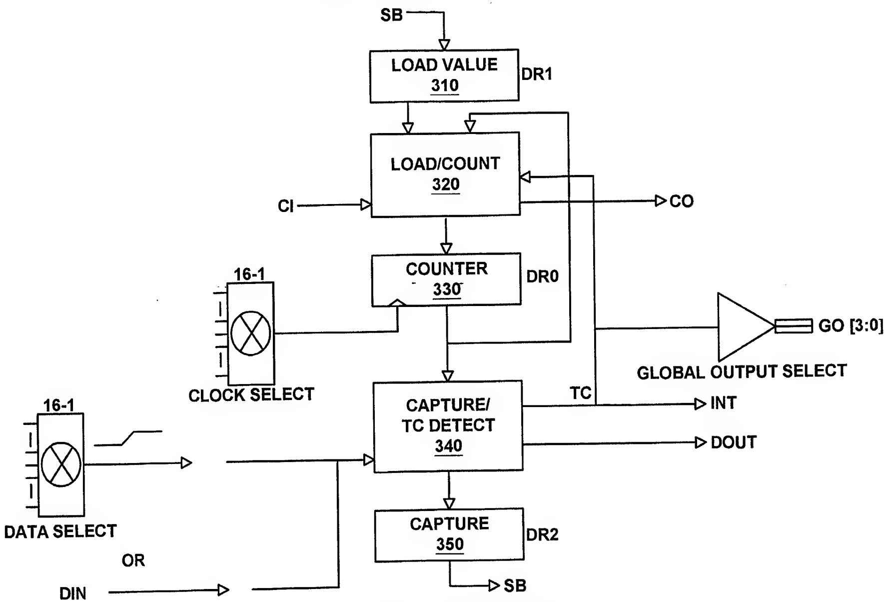


FIGURE 18

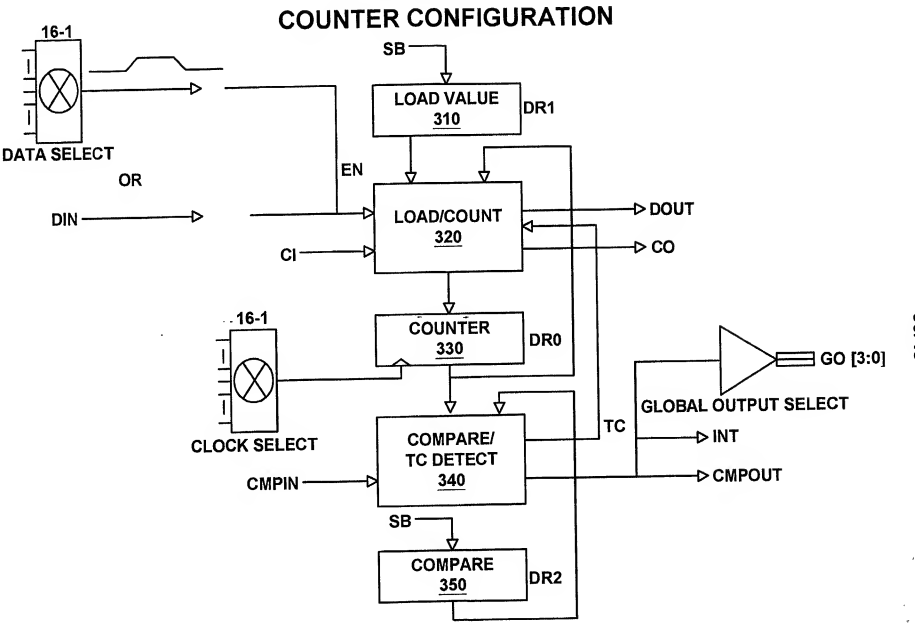

COUNTER CONFIGURATION
16-1
DATA SELECT
OR
DIN
SB
LOAD VALUE
310
DR1
EN
LOAD/COUNT
320
DOUT
CO
CI
16-1
COUNTER
330
DR0
CLOCK SELECT
GO [3:0]
GLOBAL OUTPUT SELECT
TC
INT
COMPARE/
TC DETECT
340
CMPIN
CMPOUT
SB
COMPARE
350
DR2

FIGURE 19

PWM CONFIGURATION

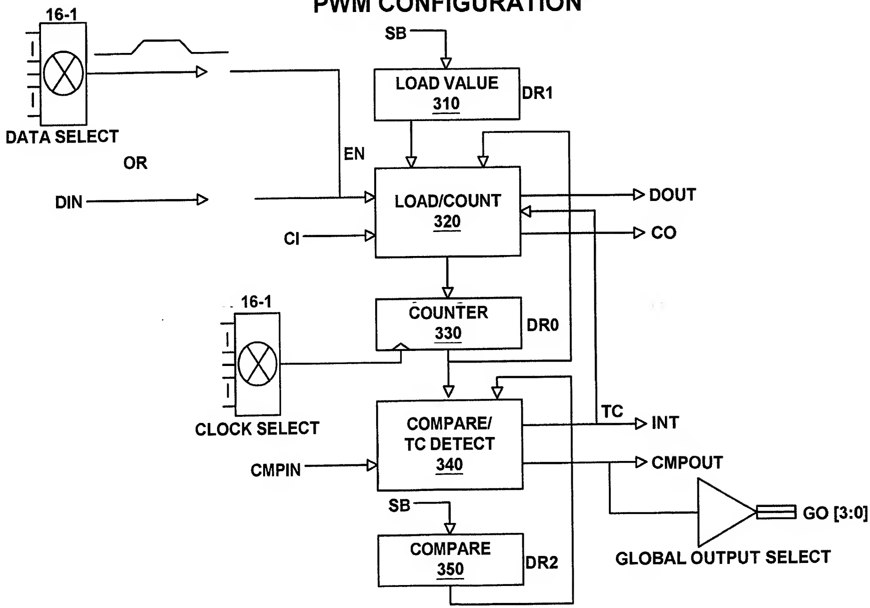


FIGURE 20

TX UART CONFIGURATION

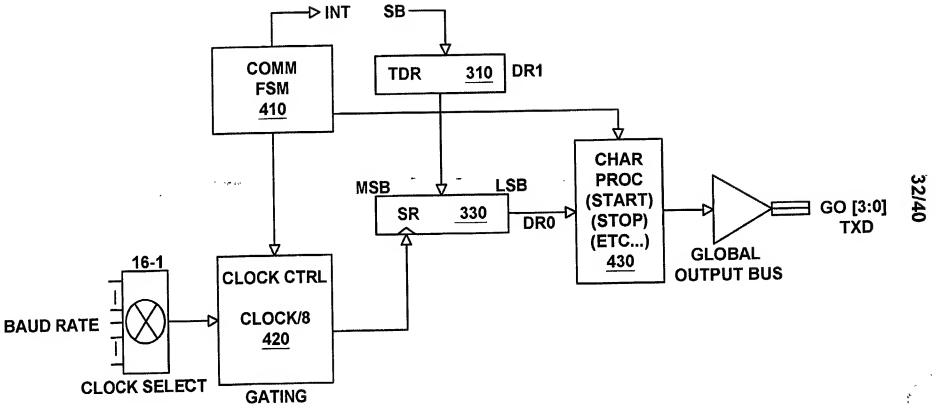


FIGURE 21

RX UART CONFIGURATION

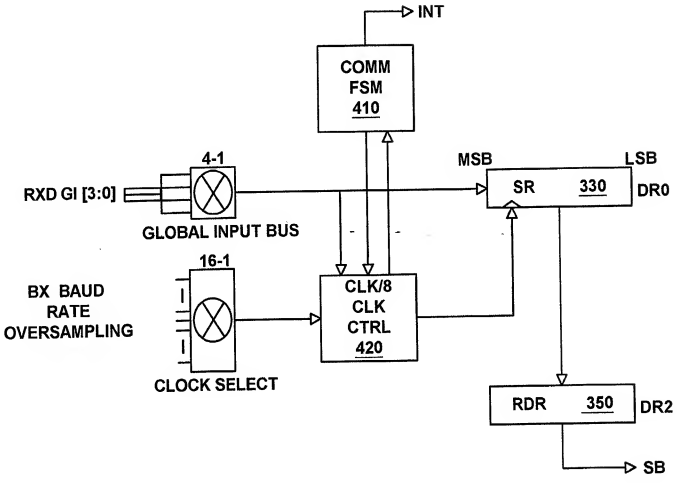


FIGURE 22

SPI MASTER CONFIGURATION

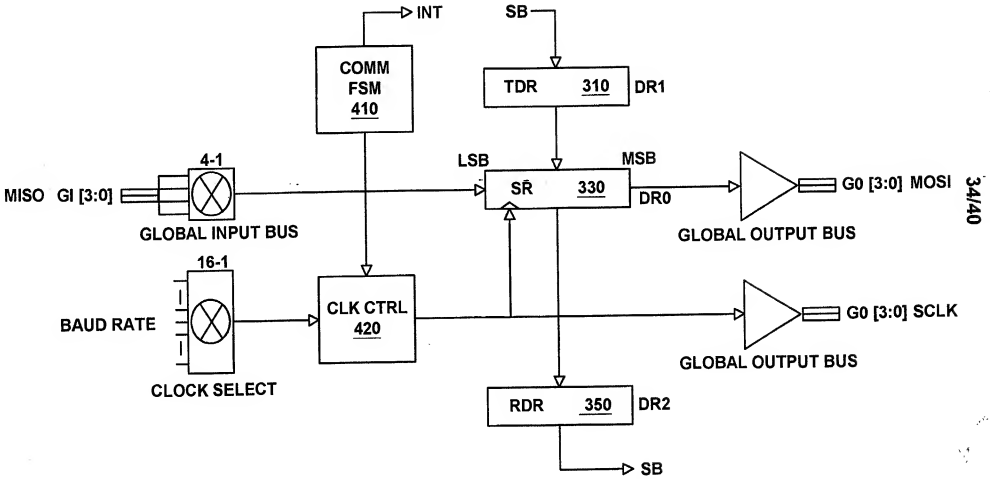


FIGURE 23

SPI SLAVE CONFIGURATION

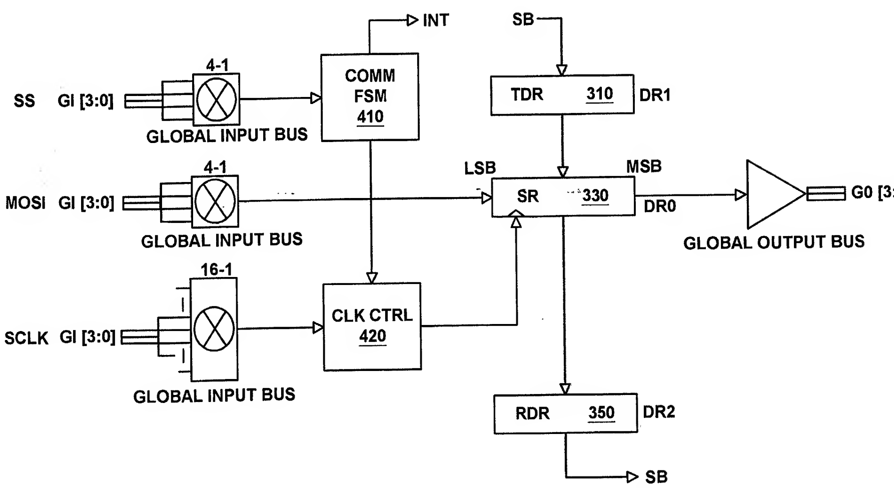


FIGURE 24

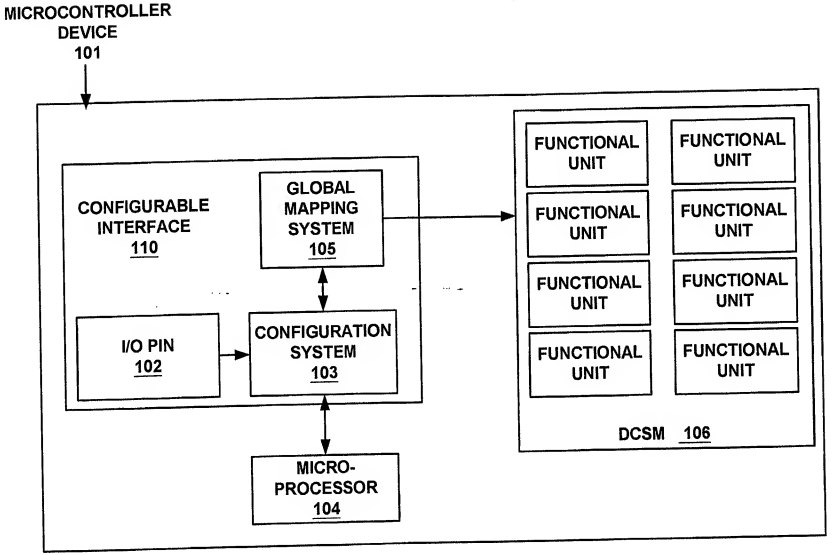

MICROCONTROLLER DEVICE 101
CONFIGURABLE INTERFACE 110
GLOBAL MAPPING SYSTEM 105
I/O PIN 102
CONFIGURATION SYSTEM 103
MICRO-PROCESSOR 104
FUNCTIONAL UNIT
FUNCTIONAL UNIT
FUNCTIONAL UNIT
FUNCTIONAL UNIT
FUNCTIONAL UNIT
FUNCTIONAL UNIT
FUNCTIONAL UNIT
FUNCTIONAL UNIT
DCSM 106

FIGURE 25

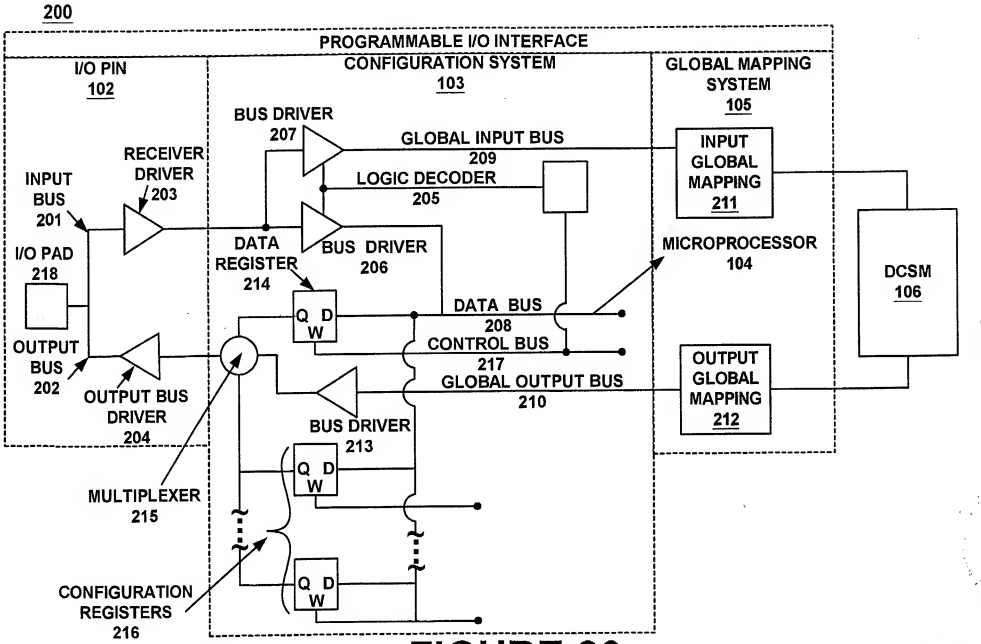

200
PROGRAMMABLE I/O INTERFACE
I/O PIN
102
CONFIGURATION SYSTEM
103
GLOBAL MAPPING SYSTEM
105
BUS DRIVER
207
GLOBAL INPUT BUS
209
INPUT GLOBAL MAPPING
211
RECEIVER DRIVER
203
INPUT BUS
201
LOGIC DECODER
205
I/O PAD
218
DATA REGISTER
214
BUS DRIVER
206
MICROPROCESSOR
104
DCSM
106
Q D W
DATA BUS
208
OUTPUT BUS
202
CONTROL BUS
217
OUTPUT GLOBAL MAPPING
212
GLOBAL OUTPUT BUS
210
OUTPUT BUS DRIVER
204
BUS DRIVER
213
MULTIPLEXER
215
CONFIGURATION REGISTERS
216

FIGURE 26

300

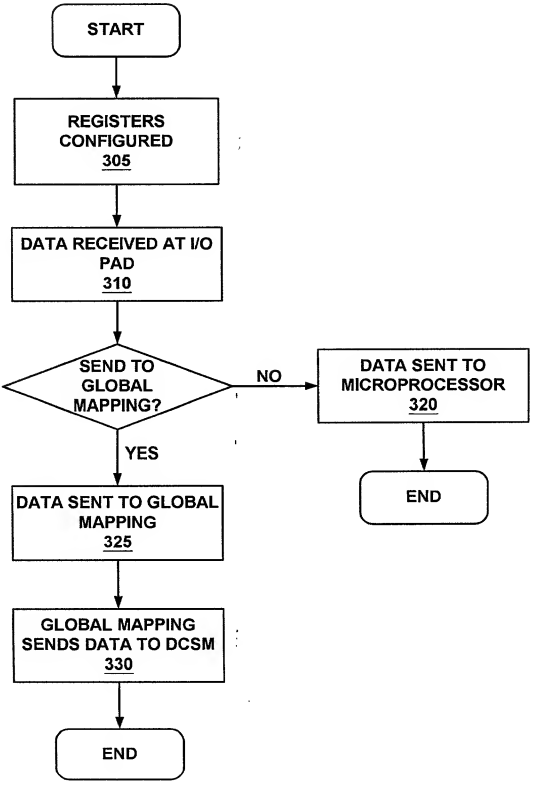


FIGURE 27

400

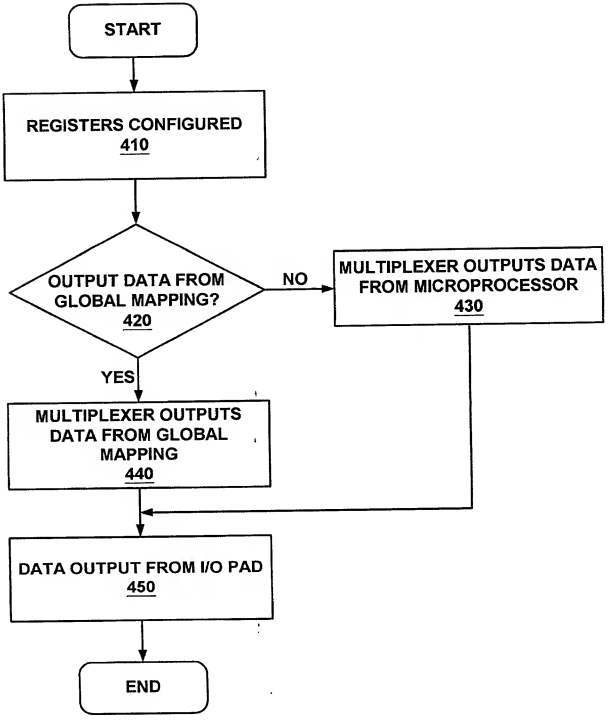


FIGURE 28

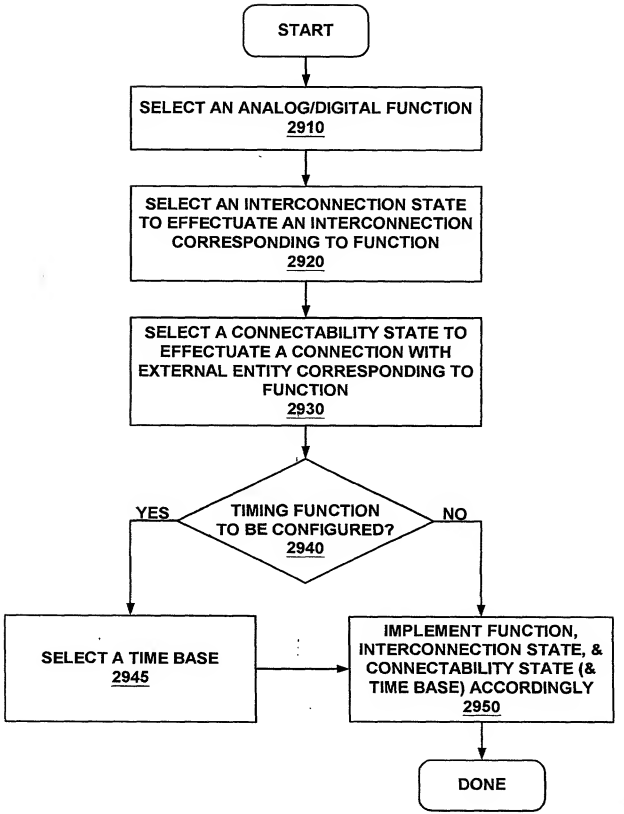


FIGURE 29